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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,066	06/24/2003	Satoshi Matsuda	008312-0304355	1198

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,066	MATSUDA ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,5,6,8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,6,8 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06242003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group I claims, comprising Claims 2, 5, 6, 8, and 10, in Letter of 08 September 2004 is acknowledged.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2 and 5 are rejected under 35 U.S.C.103(a) as being unpatentable over Yu (US 6,399,469 B1) in view of Shell et al. (US 5,429,956).

4. Regarding Claim 2, Yu discloses a semiconductor device comprising:

a semiconductor substrate (204) (Figure 8),

a pair of first diffusion layers (242,244) formed within said semiconductor substrate,

a gate insulating film including a first insulating film portion (230) formed on that portion of said semiconductor substrate which is positioned between said first diffusion layers (242,244) and a second insulating film portion (bottom part of 238, next to substrate) positioned on both edges of said first insulating film portion (230), a thickness of said second insulating film portion being larger than a thickness of said first insulating film portion,

a gate electrode (220) formed on said gate insulating film (230), and

a gate side wall insulating film (236) formed on a side surface of said gate electrode and on

a side surface of said second insulating film portion.

Yu does not disclose the presence of a second diffusion layer formed apart from said first diffusion layers within that portion of said semiconductor substrate positioned below said first insulating film portion. Shell et al. disclose the formation of a diffusion layer (40) (Figure 9) formed apart from said first diffusion layers (62) within the region below the insulating film
It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the implant procedures of Shell et al. with Yu to produce a device with improved circuit performance (Shell et al. Col. 3, lines 62 – 67).

5. Regarding Claim 5, Yu discloses a semiconductor device comprising a pair of extension regions (232,234) formed below said gate side wall insulating film, and a pair of source-drain regions (242,244) formed in contact with said extension regions (232,234).

Yu does not disclose the presence of a second diffusion layer, as discussed above, and does not disclose that the extension regions are apart from said second diffusion layer. Shell et al. disclose that the extension regions (60) are apart from the second diffusion region (40). Additionally, Yu does not disclose that source-drain regions are formed on a side opposite the second diffusion region. Shell et al. discloses that the source-drain regions (62) are on a side opposite the second diffusion region (40). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the implant procedures of Shell et al. with Yu to produce a device with improved circuit performance (Shell et al. Abstract) without increasing junction capacitance.

6. Claims 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Shell et al., as applied to Claims 2 and 5, and further in view of Chang et al. (US 5,838,044).

7. Regarding Claim 6, Yu discloses a gate side wall structure wherein a third side wall portion (236) is formed on the side surface of said gate electrode and on the side surface of said second insulating film portion (238).
Yu does not disclose a fourth side wall portion formed on a side surface of said third side wall portion. Chang et al. disclose the formation of an insulating layer (300) (oxide) (Figure 9) wherein the layer is formed on a side surface of the underlying spacers (32). It would have then been obvious to one of ordinary skill in the art to combine Mehta with Yu to obtain a device with a protective dielectric layer.

8. Regarding Claim 8, Yu does not disclose the presence of an interlayer insulating film formed to surround said gate side wall insulating film with an upper surface substantially equal to an upper surface of said gate electrode. Chang et al. disclose the presence of an interlayer insulating film (300, center) formed to surround the gate side wall insulating film (32) with the upper surface of the film substantially equal to an upper surface of the gate electrode. It would have been obvious to one of ordinary skill in the art to combine Mehta with Yu to obtain a device with a protective dielectric layer.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Shell et al., as applied to Claims 2 and 5, and further in view of Kizilyalli (US 5,767,557).

10. Regarding Claim 10, Yu does not disclose the presence of a second diffusion layer of opposite conductivity type than the substrate. Kizilyalli discloses the presence of a second diffusion layer, wherein the conductivity (p) (Col. 3 lines 35 – 38) is opposite to the conductivity (n) of the substrate (Col. 3, lines 12 –15). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kiziyalli with Yu to obtain a device with improved short channel characteristics.

Conclusions

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
November 18, 2004